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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/674,864	03/30/2001	Thomas B. Brightman	MOTOR001.001	5622

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EXAMINER	
EL HADY, NABIL M	

ART UNIT	PAPER NUMBER
2152	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/674,864	BRIGHTMAN ET AL.	
	Examiner	Art Unit	
	Nabil M. El-Hady	2152	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/8/2005 has been entered.

2. Claims 14-23 are pending in this application.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 14-16 are rejected under 35 U.S.C. 102(e) as being anticipated by and/or rejected under 35 U.S.C. 103(a) as being unpatentable over Hansen et al. (US 5,794,060), hereinafter "Hansen".

5. Hansen et al. is cited by the examiner in a previous office action.

6. As to claim 14, Hansen discloses the invention substantially as claimed including an integrated circuit constructed on one chip (Fig. 6, col. 11, lines 47-54; Fig. 19; col. 26, lines 52-5; and col. 27, lines 16-25) comprising: a plurality of data stream inputs and/or outputs that receive and/or transmit streams of data (14, 16, 18, 28, Fig. 1; 132, 136, 140, 144, 146, Fig. 7; and 216, Fig. 19); a plurality of data stream processors that process the streams of data, each data stream processor being coupled to a data stream input and/or data stream output (12, Fig.

18(a)-(c); 12, Fig. 7; PROCESSOR12, and I/O 216, Fig. 19; and col. 25, lines 54-56) and each data stream processor processing a stream of data from the data stream input and /or output the data stream processor is coupled to as the data stream is received from the data stream input and/or transmitted to the data stream output (Fig. 18c), and each data stream processor including a writeable instruction memory containing instructions (INSTR"N BUFFER CASCHE 118, Fig. 7; 32 KBYTE I-CACHE118, Fig. 19; col. 16, lines 54-59; and col. 27, lines 54-60) and a control data processor that controls the data stream processor by sequentially executing instructions from the writeable instruction memory (ETLB & TAGS 122, and Fig. 7; MMU 122, Fig. 19.)

7. As to claim 15, Hansen discloses the control data processor is a general-purpose microprocessor that has an industry standard architecture, whereby programs for the control data processor may be developed using standard tools for the architecture (col. 16, lines 1-14).

8. As to claim 16, Hansen discloses the streams of data include a serial streams and a parallel stream (col. 17, lines 18-21).

9. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hansen in view of Kolchinsky (US 5,535,406).

10. Kolchinsky is cited by the examiner in a previous office action.

11. As to claim 17, Hansen does not disclose an aggregator for aggregating certain of the data stream processors to cooperate in processing a stream of data. Kolchinsky, on the other

hand, discloses aggregating certain of the data stream processors to cooperate in processing a stream of data (col. 10, lines 30-42; and Figs. 3-6) including configurable interconnections between the aggregated data stream processors (Figs. 3-5); a configurable operation coordinator that coordinates operation of the aggregated data stream processors (configuration controller 32, and Virtual Processor Module Controller 30; Fig. 7) and a writeable configuration that specifies the configurable interconnections and the configurable operation coordinator as required to aggregate the data stream processors (configuration memory 33, Fig. 7). It would have been obvious to one skilled in the art at the time of the invention to combine the teachings of Hansen and Kolchinsky because Kolchinsky's use of aggregator for aggregating certain of the data stream processors to cooperate in processing a stream of data would enhance the functionality of Hansen system by allowing a configurable logic to offer a new mixture of performance and versatility (see, Kolchinsky, col. 1, lines 50-60).

12. Claim18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hansen in view of Murata et al. (US 6,216,179), hereafter "Murata".

13. Murata et al is cited by the examiner in a previous office action.

14. As to claim 18, Hansen discloses the integrated circuit may be used with a plurality of transmission protocols (Figs. 1 and 2). However, Hansen does not disclose a writeable configuration specifier for specifying a configuration of the data stream inputs and/or outputs. Murata, on the other hand, discloses a writeable configuration specifier for specifying a configuration of the data stream inputs and/or outputs (col. 10, lines 19-34). It would have been obvious to one skilled in the art at the time of the invention to combine the teachings of Hansen

and Murata because Murata's use of configuration specifier for specifying a configuration of the data stream inputs and/or outputs would enhance the functionality of Hansen system by allowing a configurable logic to offer a new mixture of performance and versatility.

15. Claims 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hansen in view of Deb et al. (US 6,172,990), hereafter "Deb".

16. Deb et al. is cited by the examiner in a previous office action.

17. As to claim 19, Hansen does not disclose the data stream processor further comprising a receive processor and/or a transmit processor. Deb, on the other hand, discloses the data stream processor further comprising a receive processor that operates under control of the control data processor to process the data stream received from the data stream input and/or a transmit processor that operates under control of the control data processor to process the data stream for output to the data stream output (Fig. 8; and col. 21, lines 30-67). It would have been obvious to one skilled in the art at the time of the invention to combine the teachings of Hansen and Deb because Deb's use of receive and/or transmit processor would enhance the functionality of Hansen system by providing dedicated processing for the different requirements of the receive and transmit processing.

18. As to claim 20, Hansen discloses each of the processor (working as receive or transmit processor) comprises a writeable instruction memory containing instructions (INSTR"N BUFFER CASCHE 118, Fig. 7; 32 KBYTE I-CACHE118, Fig. 19; col. 16, lines 54-59; and col. 27, lines

54-60); and the processor sequentially executes certain of the instructions to process the data stream (col. 16, lines 1-14, 54-66).

19. As to claim 21, Hansen discloses the processor (receive and/or transmit) have a plurality of processing components and are configurable to bypass one or more of the components in processing the data streams (col. 11, lines 24-32; and Figs. 5 and 6).

20. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hansen and/or Hansen in view of Deb, and/or Hansen in view of Kolchinsky , and/or Hansen in view of Murata, and further in view of Yajima (US 5,809,176) in accordance with the multiple dependency of the claim.

21. Yajima is cited by the examiner in a previous office action.

22. As to claim 22, Hansen, Deb, Kolchinsky, and Murata do not disclose a context processor to produce information about given data stream's context. Yajima, on the other hand, discloses a context processor that responds to information received from a given data stream processor that is processing a data stream to produce information about the given data stream's context and provide the context information to the given data stream processor, the given data stream processor using the context information to process the data stream (col. 5, lines 41-48).It would have been obvious to one skilled in the art at the time of the invention to combine the teachings of Hansen, Hanson and Deb, Hanson and Kolchinsky, or Hanson and Murata; and Yajima because Yajima's use of a context processor would enhance the functionality of the

produced system by speeding up the processing of the data stream in the data stream processor as a result of providing information about stream context.

23. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hansen in view of Deb, or Hansen in view of Kolchinsky and further in view of Deb, or Hansen in view of Murata and further in view of Deb, in accordance with the multiple dependency of the claim.

24. As to claim 23, Hansen, Kolchinsky, and Murata do not disclose the detailed components of the integrated system for data stream transmission. Deb, however, discloses a stream of data contains control data and payload (col. 19, lines 59-67); a received stream of data is processed in a receiving data stream processor to extract the control data and the payload (RECV Stream Proc 114b, Fig. 8; and col. 21, lines 35-37) and a transmitted stream of data is processed in a transmitting data stream processor to add control data to the payload (XMIT Stream Proc 114a, and Encapsulated Packet, Fig. 8); a buffer manager coupled to the data stream processors that provides addresses of buffers for storing payload and responds to a write operation with a buffer address to write payload to the addressed buffer and to a read operation with a buffer address to read payload to from the addressed buffer (FIFO CONTROLLER 110, 112, Fig. 2A); and a queue manager coupled to the data stream processors that manages queues of descriptors of payload, each descriptor including at least a buffer address, the queue manager responding to an enqueue command by enqueuing a descriptor provided with the command to a queue specified in the command and responding to a dequeue command by dequeuing a descriptor from the queue specified in the command (Queue FIFO 106, 108, Fig. 2A), a data stream processor responding to a received stream of data by performing a write operation to the buffer manager with the received data stream's

payload and an address provided by the buffer manager and performing an enqueue operation with a descriptor containing the address and transmitting a stream of data by performing a dequeue operation, using the address in a descriptor obtained as a result of the dequeue operation in a read operation to the buffer manager, producing a data stream using the payload received from the buffer manager, and transmitting the produced data stream (STREAM PROCESSOR, 1141, 114b, Fig. 2A). It would have been obvious to one skilled in the art at the time of the invention to combine the teachings of Hansen, Hanson , Hanson and Kolchinsky, or Hanson and Murata; and Deb because Deb's use of a buffer manager, a queue manager with the data stream processor would enhance the functionality of the produced system by speeding up the processing of the data stream in the data stream processor as a result of managing the buffering and the queuing system.

25. Applicant's arguments filed 10/1/2004 have been fully considered but they are not persuasive.

26. In the remarks, applicants argued in substance that (1), Hansen does not contemplate an implementation in which there is more than one data stream processor on a chip, (2), processor 100 in Hansen does not process a stream of data from the data stream input and/or output the data stream processor is coupled to as the data stream is received from the data stream input and/or transmitted to the data stream output, (3), Hansen's media processor 12 does not have an industry-standard architecture, (4) Kolchinsky discloses only one VPM, it can necessarily disclose nothing about aggregating a plurality of data stream processors, (5), Murata discloses nothing whatever about anything like claim 18, (6), Deb's system shows nothing equivalent to applicant control data processor, (7) context information in Yajima has

nothing to do with context information claimed, (8), Deb stores the data structure for the information about the packet with the packet and not in a separate queue.

27. Examiner respectfully traverses applicants' remarks.

28. As to point (1), in response to applicant's arguments, the recitation "constructed on one chip" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

29. Also, a ingle chip having multiple processors is not new to one skilled in the art at the time of invention. Bonneau, Jr. et al. (US 5,701,507) discloses a method of manufacturing integrated circuits uses an architecture having multiple processors and multiple memories (abstract).

30. As to point (2), Hansen's Fig. 7 discloses processor 12 as a whole with its core execution unit 100 and other components of processor 12. Processor 12 in Hansen does process a stream of data from the data stream input and/or output the data stream processor is coupled to as the data stream is received from the data stream input and/or transmitted to the data stream output. Hansen execution unit 100 is part of each of the plurality of the data stream processors. The data stream processors receive, process, and transmit data streams as claimed (col. 8, lines 45-48; and col. 27, lines 29-30).

31. As to point (3), Hansen's media processor 12 is a general purpose processor and is not a specialized one as clearly disclosed in (col. 3, lines 27-31, 58-60), which indicates that it has an industry-standard architecture.

32. As to point (4), Kolchinsky does disclose the aggregator of claim 17. The VPM controller 30 plays the role in aggregating the PPE's and their interconnections in several hardware configurations to be implemented as shown in Fig. 3 through Fig. 6 to allow flexibility in processing modes (col. 10, lines 30-42; and Figs. 3-6). It is worth mentioning also that the dynamic portioning of Hansen to allocate the appropriate amount of processing for the media stream (col. 11, lines 28-31) reads on the claimed aggregation of the data stream processors so that the aggregated data stream processors cooperate in processing a stream of data.

33. As to point (5), the limitation of a plurality of transmission protocols is disclosed by Hansen, as Figs. 1 and 2 of Hansen show clearly the use of different transmission protocols. Murata's relevancy relates to its disclosure of the second limitation of a writable configuration specifier for specifying configurations of the data stream inputs and/or outputs (col. 10, lines 19-34). The data stream is configured to include information indicating whether the job can be distributable processed or not among clusters of processors (see col. 9, line 62 to col. 10, line 34).

34. As to point (6), Deb is cited by the examiner to show that concept of using separate transmit stream processor and receive stream processor is not new in the art. Deb's teachings

are combined to the teachings of Hansen which uses a control data processor with writable instruction memory to control the operation of the data stream processor.

35. As to point (7), Yajima is cited by the examiner to show that the concept of using a context processor is not new in the art. Yajima discloses a context generator that responds to information received from a given data stream processor to produce information about the given data stream context and provide the context information to the given data stream processor (col. 5, lines 16-22,41-48).

36. As to point (8), Although Deb discloses storing the data structure for the information about the packet with the packet, he stores pointers to portions within the packet data that may be of interest to upper layer protocol or portions of data that may be quickly read and processed without having to spend CPU bandwidth to scan and process the entire packet (col. 11, lines 25-35). Deb also discloses in another embodiment that the data structure information may be provided in the form of a descriptor of payload that is then processed (col. 11, lines 39-42). It would have been obvious to one skilled in the art at the time of the invention that the data structure information provided in the form of a descriptor and not appended to the payload is a design choice and would have been managed by the queue manager.

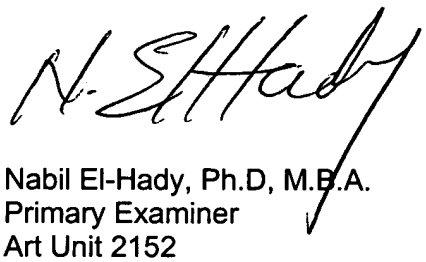
37. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Flaig et al. (US 5,105,424) ; Bonneau, Je. Et al. (US 5,701,507) ; Elliott et al. (US 5,546,343) ; Wright et al. (US 6,195,739); Tremblay et al. (US 6,205,543); and Luijten et al. (US 6,324,164).

38. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nabil M. El-Hady whose telephone number is (571) 272-3963. The examiner can normally be reached on 9:00 - 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on (571) 272-3964. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



September 19, 2005

Nabil El-Hady, Ph.D, M.B.A.
Primary Examiner
Art Unit 2152